SYNOPSYS®

DATASHEET

TestMAX Diagnosis

Fast and Accurate Silicon Defect Isolation

Unparalleled throughput for high resolution and accuracy of silicon defect candidate selection

Overview

Synopsys TestMAX Diagnosis analyzes defective silicon results to determine the corresponding defect locations. It delivers unparalleled runtime, ensuring high accuracy of silicon defect candidates for failure analysis.

TestMAX Diagnosis complements TestMAX ATPG and utilizes the same design database.

Key Benefits

- Quickly finds silicon defect candidates for failure analysis
- Fast startup with reuse of TestMAX ATPG design image
- High throughput with parallel diagnostics of multiple fail logs
- Isolation of systemic defects with volume diagnostics supported by Yield Explorer

Key Features

- Highly optimized, memory-efficient analysis and fault simulation engines for order of magnitude faster diagnostics run time
- Fine-grained multithreading across multiple cores overcomes memory bottlenecks
- Identical diagnostic results across different server configurations, machines, and core use for consistent analysis
- Physical diagnostics for accurate defect isolation
- Integration with the database for TestMAX ATPG for consistent results
- Advanced fault models for high resolution and accuracy: standard and slack-based transition, cell-aware, static/dynamic bridging, path delay, and hold-time

Introduction

Scan-based design-for-test (DFT) is now the standard digital logic testing methodology for almost all SoC designs. Scan-based DFT provides another equally significant benefit: the same infrastructure enables a highly automated and accurate process for not only identification of defective devices, but also for identifying the specific location of the processing defects that caused it to fail. While the basic goal of delivering fully functional parts only requires stop-on-first-failure testing, further testing of failing devices can provide useful, detailed information as to why the part failed. When this data is collected and analyzed over a significant volume of failing parts, systematic issues causing lower manufacturing yields can be statistically separated from the "noise" of random defects. Correlating the defect locations from a large number of devices, prioritizing those with the highest yield impact, and taking immediate corrective action has enormous potential cost benefits. and enables faster time to market when new designs are being ramped up in manufacturing. This first step in the process starts with diagnostics of a single failed die with TestMAX Diagnosis.

Unparalleled Diagnosis Runtime and Throughput

Yield ramp for increasingly complex SoC designs and shrinking market windows requires fast diagnostics turnaround time. TestMAX Diagnosis overcomes this bottleneck using state-of-the-art diagnostics engines (Figure 1) that are extremely fast, exceedingly memory-efficient, and highly optimized for fine-grained multithreading of diagnosis processes across multiple cores. For increased throughput, TestMAX Diagnosis processes multiple fail log files concurrently, with each diagnostic job sharing the same image for specific configurations, resulting in more diagnosis results with less memory.

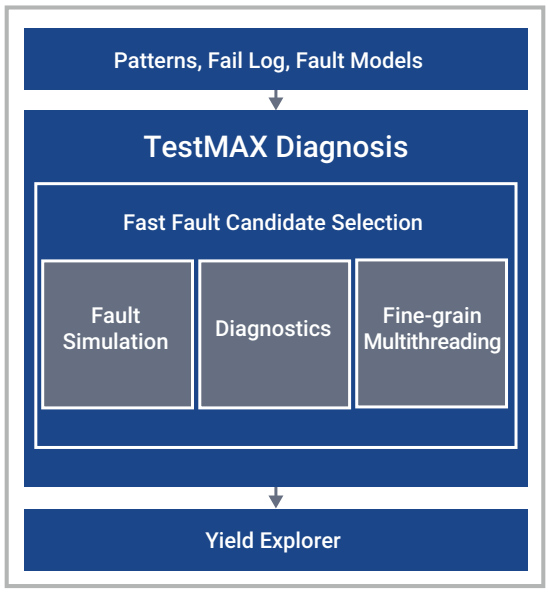

Figure 1: TestMAX Diagnosis uses state-of-the-art diagnostics engines

Physical Diagnostics

Automatic and accurate defect isolation is an important step in diagnosing critical yield issues, both during production ramp and in volume manufacturing. In addition to identifying defective parts from manufacturing, TestMAX Diagnosis uses physical information about a design to quickly isolate the location of defects in devices that fail ATPG patterns. It reads the test patterns and tester failure data, which are the differences between measured and expected responses to those test patterns, and reports the fault candidate locations that most likely explain the faulty device behavior observed on the tester. TestMAX Diagnosis uses advanced heuristics and a high-performance fault simulator for rapid and reliable results in a volume manufacturing environment.

To perform volume diagnostics and yield analysis, Synopsys Yield Explorer® directly reads diagnostics results from TestMAX Diagnosis and loads them into a complete database of previous diagnostics results, other test data, multiple domains of design data, and if available, process data from the fab (Figure 2). Yield Explorer then correlates the diagnostics results with specific failure mechanisms to determine the key design or systematic issues contributing to yield loss.

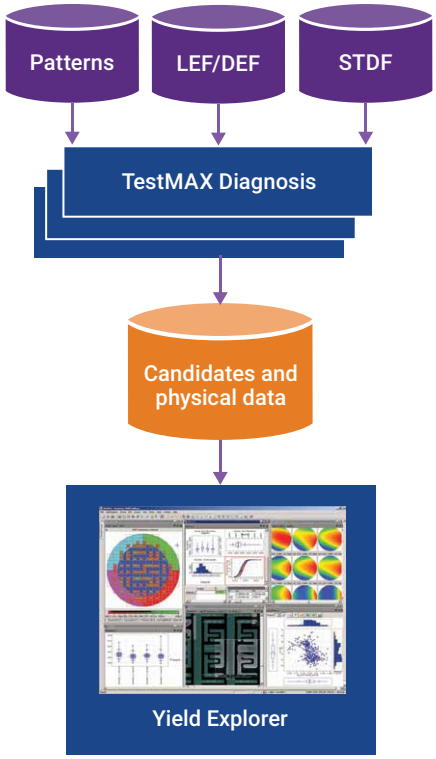

Figure 2: TestMAX Diagnosis works with Synopsys Yield Explorer to perform volume diagnostics and yield analysis

Cell-Aware Diagnostics

To provide future defect isolation within a library cell, TestMAX Diagnosis supports the use of cell-aware fault models. These fault models are created with utilities for TestMAX ATPG. Once available, cell-aware fault models are utilized on any type of TestMAX ATPG patterns and not limited to cell-aware test patterns. The defect search area within the cell is often reduced by 3-5X compared to standard diagnostic techniques (Figure 3). The result is faster turn-around time for physical failure analysis.

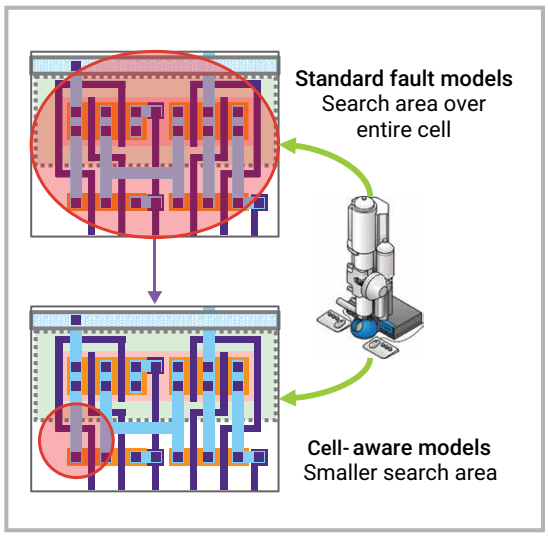

Figure 3: Cell-aware fault models reduce defect search area within the cell compared to standard diagnostic techniques

Tight Links with Synopsys Tools

- Reads TestMAX ATPG scan patterns and TestMAX XLBIST patterns
- Integrated with Yield Explorer for seamless volume diagnostics and yield analysis to uncover design and process issues causing yield loss
- Leverages Synopsys cell-aware fault models (optional)

Netlist and Test Pattern Formats

TestMAX Diagnosis supports the same industry standards for data formats, simulation testbenches, and tester interfaces:

- Circuit netlist: Verilog, VHDL (1987 and 1993)
- Library: Verilog functional (Structural and UDPs)
- Design layout: LEF/DEF interface
- Test Patterns: STIL, WGL, Verilog
- Tester fail log formats: STDF (V4 and V4-2007)